# Fabrication of HEMT Structures, with Extension to the Study to Zero/One-Dimensional Structures Fabricated Using an Electron Beam Lithography System

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ABSTRACT

Technological developments over the last few decades have created the possibility to fabricate electronic devices on a nano-meter scale. The physics of these small devices is dominated by quantum mechanics. In this project, two dimensional electron gas and one dimensional electron gas samples were fabricated and measured. The project work involved a thorough analysis and explanation of the electron transport in such mesoscopic systems, covering the fundamental characteristic effects observed in these systems, such as the Quantum Hall effect in the 2D systems and the quantized conductance effect in quasi-1D devices.

Keywords: Quantum Hall Effect; Low-dimensional semiconductor heterostructures; Quantized resistances and conductance; Electron Beam Lithography (EBL); Split-gate devices; 1D channel

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## INTRODUCTION

Nanotechnology has been a challenging research area because of the fabrication and processing carried out for developing meso-scopic systems; however this is extremely rewarding because of the dimensionality playing an important role in determining the properties of materials, for example the ways of electron interactions in three-dimensional, two-dimensional (2D) and one-dimensional (1D) structures [1-3]. Major advances in lithographic technology have enabled researchers to fabricate nano-scale structures which have great control over electron transportation. For performing quantum observations of low-dimensional electron transport, firstly one has to make sure the thermal energy is less than the electron energy-level spacing which is achieved by combination of temperatures less than 1 K (-272 $^{o}$C) and device dimensions less than one micron. Secondly, motion of electron must be ballistic, meaning no scattering of electrons within the transport medium [4]. Among different quantum devices, simplest is a two-dimensional electron gas where the electron gas (2DEG) is confined in one direction and is free in the other two. This confinement is achieved by forming *heterojunctions* between two different band gap semiconductor lattices. Most common and widely explored of all is GaAs/AlGaAs (1.42 eV and 2eV respectively) heterojunction structures because of the potential of high mobilities that can be achieved by varying growth parameters [5-8]. The band diagram of a two-dimensional heterostructure is as shown in Figure 1; from the band diagram one can see that due to low-confinement, the electrons occupy discreet energy bands called 'sub-bands' and this results in quantized motion of electrons in a quasi-2D channel as shown by Shubnikov-de Haas Oscillations [9-10].

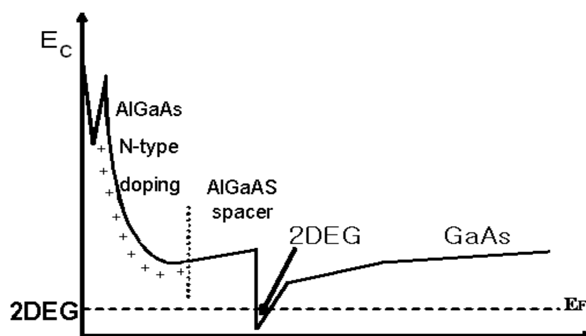



Figure 1. Band diagram of 2DEG formed

Confinement in further dimensions leads to development of nano-structures such as quantum wires and dots. This is usually achieved by patterning point contacts called Sharvin contacts [11] fabricated by electron beam lithography (EBL). When the negative bias is applied to this gates it depletes electrons from the 2DEG lying underneath the electrodes. This ballistic transport in quasi-one dimensional channel results in quantum corrections of quantized conductivity as observed in 2DEG [12].

## FABRICATION AND DESIGN

In order to form Hall Bar channel for conduction of electrons on the semiconductor mesa, pattern of Hall Bar onto the substrate needs to be developed. This is done by

implementing time-efficient optical lithography process which in this case is used for pattering large areas such as Hall Bars in first round and then Metal contacts at the terminal of Hall Bars in second round.

For patterning Hall Bar mesas negative photo resist (Shipley 1813) was spun over the wafer sample at 5000 rpm for 30 sec which gave thickness of resist deposited of 1.2 μm similar to what can be achieved in resist datasheet. This was then followed by soft bake of resist in order to improve its adhesion at 115 $^{o}$C for 60 sec. The pattern was then exposed to Ultraviolet radiation for 7 sec. The photo resist pattern was then developed by Microposit MF-319 developer for 60 sec followed by rinsing with IPA (isopropyl alcohol) and water, and is as shown in Figure 2.

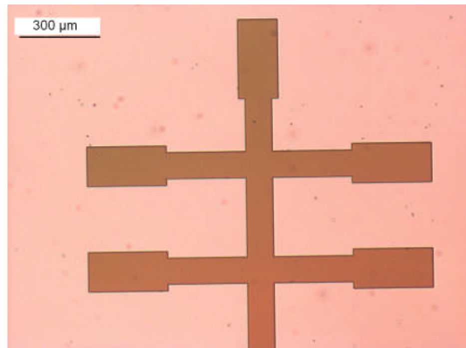


Figure 2. Hall bar patterned on photo-resist due to optical exposure

The height of the resist pattern was then measured using Alpha-Step IQ, stylus-based surface profiler.

After looking at the surface profile of the resist pattern, wet etching is followed and the etchant used during the course of project for different sample wafers was a mixture of DI (deionised) water, sulphuric acid ($H_2SO_4$) and hydrogen peroxide ($H_2O_2$). The ratio of these components and time for which samples was immersed in etching solution were crucial factors in determining the height of the sample mesa to be etched. For e.g. for one of the sample with 20 nm spacer layer, the amount of etching height needed to make direct contact with unetched 2DEG with metallic contacts is 70nm. The required etching height was achieved using etchant solution of (DI water: $H_2SO_4$: $H_2O_2$ = 160 ml: 8 ml: 1 ml) and the sample being immersed in the solution for 23 sec. This process was followed by removal of photo resist using Acetone solution and then measuring the etched profile using surface profiler. The thickness of the etched surface measured was 84 nm uniform through out the Hall Bar sample featuring four arms, compared to 70 nm 2DEG depth.

The data for the etched mesa height achieved for 20 nm, 40 nm, and 60 nm spacer layer samples and the amount of time sample was immersed in the solution for getting the required mesa height is as tabulated in Table 1.

| Sample Spacer layer | Concentration of Etchant Solution DI:H2O2:H2SO4 | Mesa Height required | Etching Height Achieved | Time for Etching |
|---|---|---|---|---|
| | | | | |
| 20 nm | 160ml : 8ml :1ml | 70 nm | ~80 nm | 23 sec |
| | | | | |
| 40 nm | 160ml : 8ml :1ml | 90 nm | ~100 nm | 25 Sec |
| | | | | |
| 60 nm | 160ml : 8ml :1ml | 110 nm | ~115 nm | 26 sec |

Table 1. Showing tabulated data of etching height achieved using same etchant solution for different time duration

One of the advantages of wet etching technique is it confines the 2DEG without any kind of contamination and also side wall damage of the mesa formed is less [13] which can ease the continuous run of split gates deposited on Hall Bar as discussed further. As the mesa is formed the only thing left now is to form metal contacts at the terminals of Hall Bar.

The metallic contacts deposited on the Hall Bar terminals should be at the same potential in order to conduct through the mesa easily and to easily measure the potential difference at different points across the Hall Bar and this is achieved by depositing Ohmic contacts at the terminals. Ohmic contacts were also patterned by optical lithography similar to first lithography process carried for mesa formation and Au/Ge/Ni alloy slugs were thermally evaporated for 200 nm metallization. While patterning contacts pads, the mask of the contact pads were aligned to the end of the Hall Bar and the four arms with extremely high accuracy and the pattern is then developed after exposing the bond pads.

While developing the contact pads area exposed, the sample was first immersed in chlorobenzene for 3 min prior to immerse in developer in order to assist lift-off process after metallization. The metallization process using thermal evaporation of the metal alloy, lift-off technique is followed by dipping samples in the acetone for ~2h and the sample with metal bond pads deposited is shown in Figure 3.

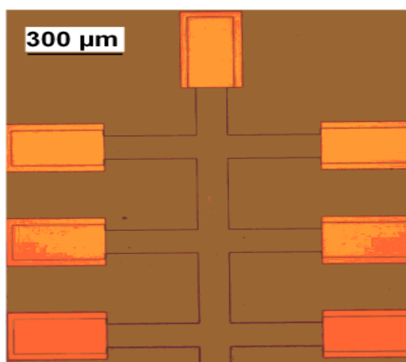



Figure 3. (Ohmic contacts processing) Hall bar pattern after lift-off process following metallization of Au/Ge/Ni alloy

In order to diffuse the Au/Ge/Ni alloy to contact the 2DEG beneath the surface, annealing technique was applied at 420 $^{o}$C for 90 sec in a reducing ambient such a

forming gas ($N_2/H_2$), which in turn improves the metal-semiconductor contact resistivity.

Finally in the last stage of HEMT fabrication the bond-pads on the Hall bar terminals were bonded on to the chip package using wire bonding. And the samples after this stage were used for Quantum Hall measurements at DC and AC frequencies for characterising samples grown at different conditions using MBE.

In order to write split-gates pattern on the Hall bar, e-beam lithography was performed using Raith-50 e-beam writer. This time instead of forming a layer of Shipley photo resist on the sample, a polymethylmethacrylate (PMMA) bilayer (495 A4) was used as a spin coated resist which was spun at 5000 rpm for 30 sec giving film thickness deposited on Hall bar of around 1800 $A^o$ which was similar to what was expected from the manufacturer datasheet. The resist coated sample was then baked at 170 $^oC$ for approximately ~ 2 hours.

E-beam lithography was then performed to write the pattern of split-gates on the Hall bar mesa, all together four pairs of gates were to be formed on the Hall bar sample. While performing this technique extreme care was taken in setting up dose parameters and exposure time for the e-beam. In order to get good exposure, these parameters should be precisely in accordance with the resist thickness deposited onto the sample; any un-uniformity in the resist thickness can result in poor exposure of the area to be patterned and can eventually result in poor metallization of gates, which was the case observed for one of the samples; poor metallization result is as shown in Figure 4.

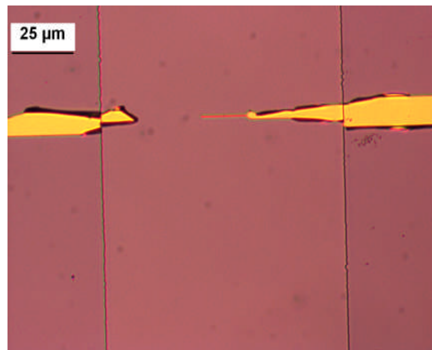


Figure 4. Poor deposition of metal on split-gates because of the unsuccessful exposure resulting from the set dose parameters not in accordance with PMMA resist thickness

After performing e-beam lithography the pattern written on the sample was then developed using standard PMMA developer solution of MIBK:IPA (1:3) for 70 sec and then the sample was rinsed in IPA for 30 sec. The spilt gates pattern with split width of 300 nm was successfully developed and is as shown in Figure 5.

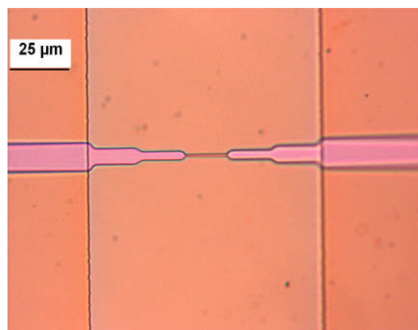


Figure 5. Successfully developed e-beam lithography from individual split-gate view

After developing the lithography carried out on the sample metal was deposited on the split-gates in order to make contacts with the bond-pads and so with negative bias source. The contacts formed at this stage are Schottky contacts in order to restrict bidirectional flow of electrons to prevent any leakage in negative bias applied to the gates. The metallization carried out consisted of thermal evaporation of 20 nm of Ti in order to provide better adhesion to the GaAs surface followed by 60 nm Au. Au was chosen for the metallization process because of the reproducible Schottky barrier which forms at the semiconductor interface. Thickness of Au was evaluated from the rule of thumb for PMMA resist, where the thickness of the metal deposited should be around one-third of the resist thickness (1800 A$^{o}$) spread for e-beam lithography. And the lift-off process during this stage will be the same as previously discussed; the only thing to note is for successful lift-off the amount of time the sample was immersed in acetone was longer around ~8-10 hours because of the small feature area patterned.

The metallic gates on the sample after this phase as observed are shown in Figure 6.

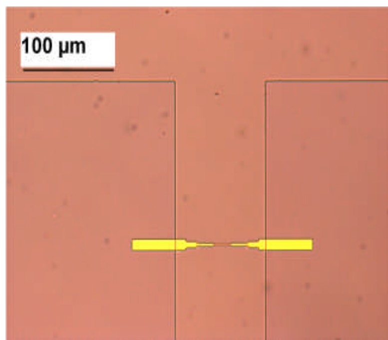


Figure 6. Successful lift-off after metallization process of Ti/Au (20 nm/60 nm) on split-gates developed using e-beam lithography from individual split-gate view

The bonding pads with larger feature area were then drawn by time-efficient conventional optical lithography process which were then developed as mentioned before and the process was then followed by metallization of the pads again to make sure that the contact formed between gates and pads was leakage free, Schottky contacts were developed using thermal evaporation of 20 nm of Ti followed by thicker layer of 100 nm Au.

At the final stage of fabrication process for split-gates devices the bonding pads were bonded onto the chip package before bonding the gates to the contacts on the package, all of the contacts on the package were shorted with bonding wires using 'stitch bonding technique' in order to prevent any generation of unnecessary charge at gates which can damage the split-gates devices. The metallic pads on the sample connecting with gates before bonding them to the package are as shown in Figure 7.

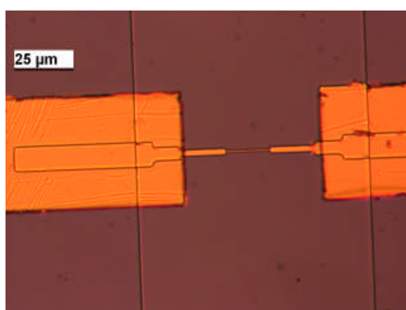


Figure 7. Successful lift-off after metallization process of Ti/Au (20 nm/100 nm) on bond pads developed using optical lithography from individual split-gate view

## Quantum Hall Measurements

For the measurements, we used an AC signal generator which supplies voltage across the Hall Bar through current limiting resistor and a couple of Lock-In amplifiers were used to read up Hall and Longitudinal voltages from the ohmic contacts on the Hall Bar. The schematic diagram of the AC Quantum Hall measurement system is as shown in Figure 8.

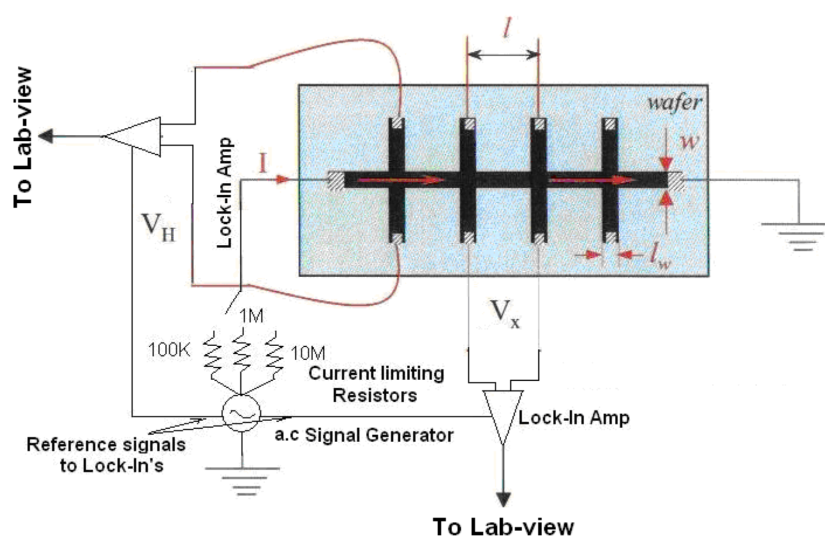



Figure 8. AC Hall measurement setup

After setting up the system, code for interacting Lock-in amps with the signal generator and magnet was developed on Lab-View software which as mentioned earlier was successfully able to control the source signal generator and to read the voltages values from the Lock-In and display it on to the screen. The program to control the temperature inside the cryostat still, however, needs some more consideration, until this time AC Hall measurements were performed by manually controlling the magnet and temperature sensors.

One of the main aspects in Quantum Hall measurements is to characterize the ballistic transport of 2DEG affected by thickening of spacer layers giving more isolation to the carriers from the doped ionized impurities as briefly discussed before. And for that reason we used samples L 270 and L 233 and L 296 grown using identical growth condition in MBE and also by using the same growing cell in MBE i.e. GaV in this case, the only difference maintained between two samples was the growth of AlGaAs spacer layer which was 20 nm, 40 nm and 60 nm respectively as referring back to HEMT structure shown in Figure 1. The evaluation of sample properties was carried out in similar way as that of discussed for DC measurements but in order to solve our previous problem of an arguably slight offset in the 0 T point, single field measurements with regards to B (T) were now carried at 0.1 T slightly away from 0 T in order to avoid impact of zero offset of the magnetic field, (and it was ensured that we didn’t go at high enough fields for the voltages to start getting quantized). After these evaluations the sample properties evaluated were double checked by analyzing samples through Shubnikov-de Haas oscillations. It was important that the frequency of the voltage applied to the Hall Bar was not in multiples of 50Hz mains as measurement results were easily affected by the mains frequency oscillations. The values of $N_s$ and μ results evaluated from single field

measurements, for constant current value of 176.75nA at AC frequencies in Hall Bar at 1.5K and at 0.1T are tabulated in Table 2.

| QHE MEASUREMENTS AT ~ 1.2K | | | | | |
|---|---|---|---|---|---|
| Wafer No. | Sample no. | SHEET DENSITY [$N_s$ ($cm^{-2}$)] | | MOBILITY [$\mu$ ($cm^2/V sec$)] | Conditions |
| | | by SdH Osc. | by LOCK-IN (current I=176.75nA, B=0.1T) | by LOCK-IN (current I=176.75nA, B=0.1T) | with info of frequency used in LOCK-IN measurments |
| | | $N_s$=(4.826E10)/Δ(1/B) | $N_s$=(I*B)/(q*$V_H$) | $\mu = R_h/\zeta_{2D}$. | |
| L233 40:40:10 with (GaV & Al1) | 1 | | 1.70E+11 | 866666.67 | Dark (f = 510Hz) |
| | | 1.65E+11 | 3.39E+11 | 1648607.59 | Light (f = 1.1kHz) |
| | 2 | 2.75E+11 | 1.53E+11 | 875378.21 | Dark (f = 510Hz) |
| | | 1.52E+11 | 3.04E+11 | 1684562.24 | Light (f = 1.1kHz) |
| | | 2.69E+11 | | | |
| L 270 20:40:10(GaV-Tip 8% &Al1)] | 1 | 3.01E+11 | 2.93E+11 | 815135.14 | Dark (f = 721Hz) |
| | | 5.09E+11 | 5.00E+11 | 1403174.60 | Light (f = 721Hz) |
| | 2 | 3.07E+11 | 2.99E+11 | 826492.25 | Dark (f = 721Hz) |
| | | 5.07E+11 | 5.05E+11 | 1423044.32 | Light (f = 721Hz) |

Table 2. AC Hall Bar measurements, with Sheet density evaluated using single point (0.1 T) and variable field (0 to 6 T) methods, mobility evaluated from single point (0.1 T) method.

Table 2 shows the characteristics of the Hall Bar samples evaluated in terms of sheet density and mobility values for L 233 and L 270 from single point field and variable field measurements. First thing to be noted from the tabulated results is the similarities in the sheet density values Ns evaluated from both using equation (2.1), (2.2), (2.3) and from Shubnikov-de Haas oscillations as shown in Figure 9 which surely confirmed the skeptical view about the zero offset in zero Tesla value.

$[N_s(cm^{-2})]=I*B/(q*V_H)$ (2.1)

$[\mu(cm^2/Vsec)]=R_h/\zeta_{2D.}$ (2.2)

$R_h$ being Hall coefficient, is $1/(q* N_s)$ and $\zeta_{2D}$ is 2D carrier sheet density between two adjacent/longitudinal contacts in Hall Bar which is defined in equation (2.3).

$\zeta_{2D}=[R_{xx}*(width,w)]/(length,L).$ (2.3)

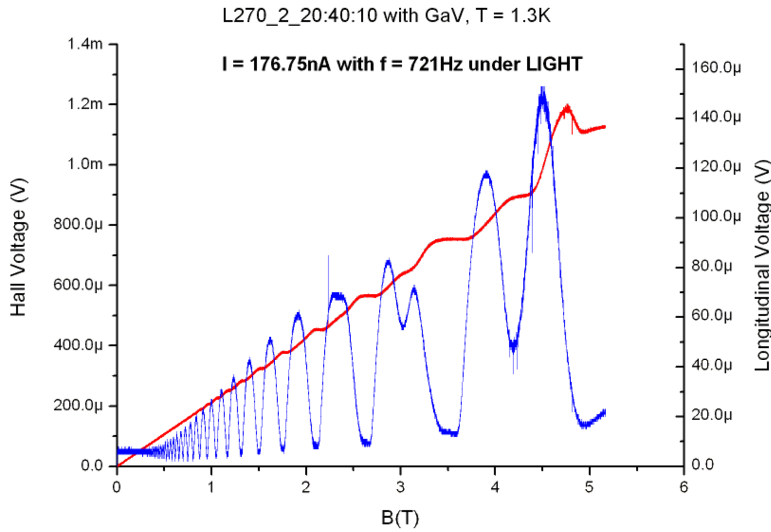



Figure 9. Shubnikov-de Haas oscillations evaluated for L 270 under illumination at 1.3 K from 0 to 6 T field, using AC Hall measurement setup

Where:
Sheet-density=[4.826E10]/Δ(1/B), (2.4)
and B is the different values of magnetic field at which longitudinal voltage in the oscillations becomes ZERO.

The measurements for L 296 were not successful because of the contacts getting frozen up at liquid helium temperatures, however it would be interesting to compare the results with the rest of the sample batch. Nonetheless, we can see for L 270, sample with thinner spacer layer has higher $N_s$ and in contrast to L 233, sample with thicker spacer layer having lower $N_s$ both under dark and illuminated conditions, as expected the thinner the spacer layer more Si electrons will penetrate into the well and so increase the carrier concentration. Also we can see a notable amount of increase in $N_s$ and so mobility values under illuminated conditions due to electrons moving into lower sub-bands. A clear picture of variation of Sheet density and mobility values for 20 nm and 40 nm spacer samples under dark and light conditions is given by the graphs as shown in Figures 10 and 11 respectively. This is what we expect, as spacer layer increases Mobility increases but the carrier concentration depletes and this trend continues until there are not enough carriers left to take part in increasing the sample mobility and so it should drop abruptly. This might be the case for us if the AlGaAs spacer layer was increased to 80 or even 100 nm.

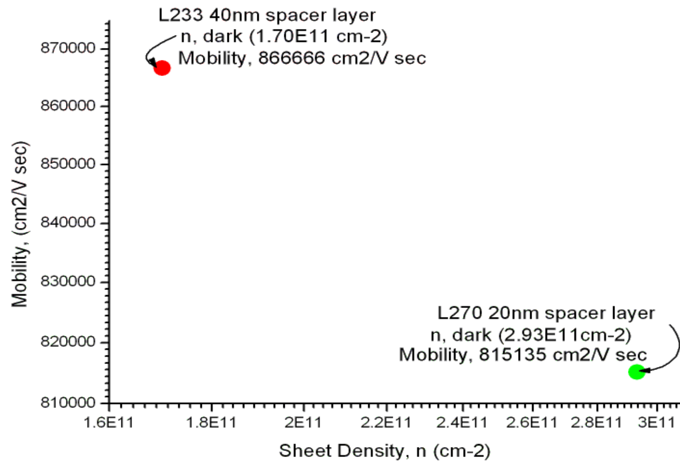



Figure 10. Sheet density and mobility comparison under Dark conditions for L 233 and L270

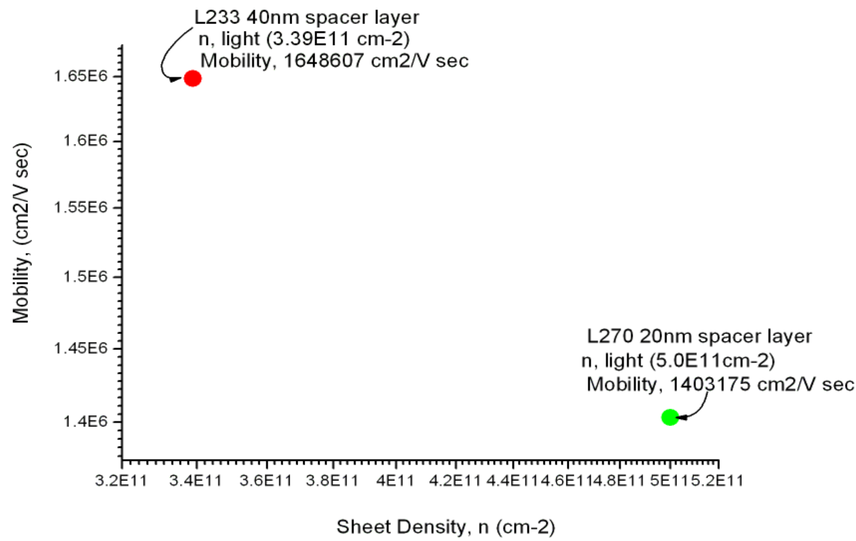



Figure 11. Sheet density and mobility comparison under Light conditions for L 233 and L 270

Another way of comparing the characteristics of the two aforementioned different spacer layer samples is as shown in Figure 12, which shows the gradient of the increase in sheet density and mobility due to illumination conditions to that of density in dark conditions for two different spacer layer samples.

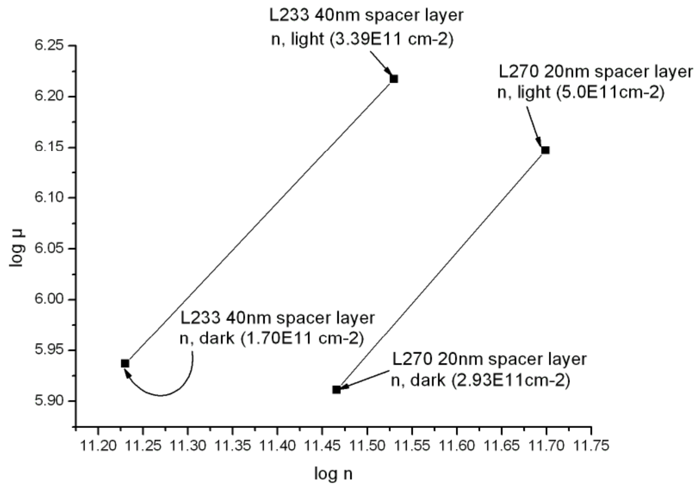



Figure 12. Sheet density and Mobility gradient

## RESULTS AND ANALYSIS

With similarities in one point measurements, Shubnikov-de Haas oscillations for the above samples were also reasonably similar under DC and AC conditions, and sheet density values evaluated from Shubnikov-de Haas oscillations for AC setup were very similar to that of measured using DC setup, e.g. of SdH oscillations comparison for L270 for two setups under light are as shown in Figure 13 and Figure 14.

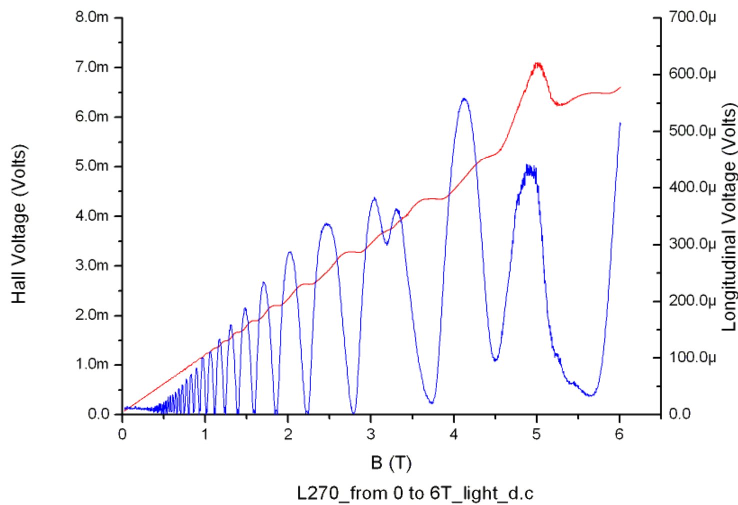



Figure 13. Shubnikov-de Haas oscillations for L 270 using DC setup

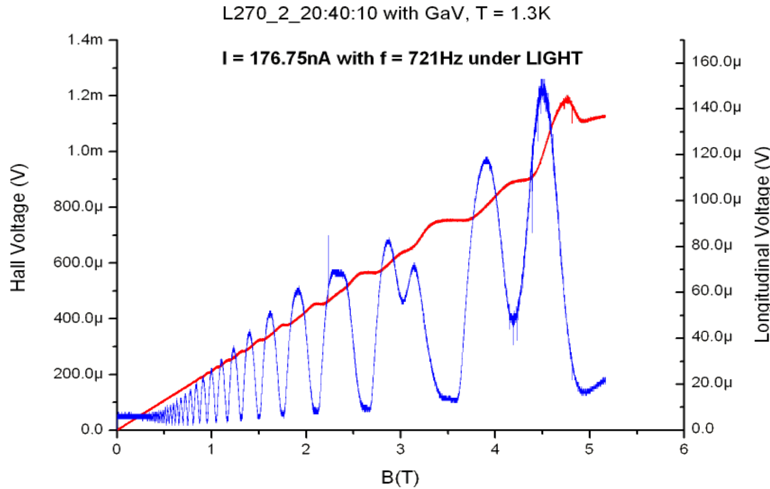



Figure 14. Shubnikov-de Haas oscillations for L 270 using AC setup

The final part of the analysis includes analyzing the plot of Hall Resistance vs B (T) where the Hall resistance scale is evaluated in terms $h/ne^2$ which varies in multiples of $h/ne^2$, so we can accurately determine at what multiples Hall Resistance is quantized between two landau levels. The plots for above samples under both conditions are as shown in Figure 15 for L 233 and in figure 16 for L 270.

## A few comments from the above plots

As we can see, the Plateaux in Hall resistance are occurring at every 1/even multiples (i.e.1/2, 1/4, ..) of $h/ne^2$ but at high fields they start occurring at every 1/n multiples (n being integer i.e. 1, 2, 3…); this is a result of Zeeman splitting of Landau levels[14]. Also we can see that n, which represents completely filled Landau levels, with neB/h electrons under Fermi energy decreases with increasing magnetic field.

With increasing magnetic field we can see the density in each Landau level increases and so to keep the sheet density constant, lower Landau levels will pass through the potential. Increase in spacing between these levels results in oscillation of Fermi-energy with period of 1/B.

In addition note that as we illuminate the sample, the carrier concentration in the sample increases which will increase the number of filled Landau levels inside the Fermi energy, as a result we can see from the plot of above samples under illumination, the multiples of $h/ne^2$ at which Hall Resistance is quantized are much smaller than that under Dark conditions of same sample at same temperature and so we can say that slope of the Hall resistance plot decreases as the sample is illuminated. From the above results we were unable to see Quantized Hall Plateaux at $1*(h/e^2)$, for that, we need to go to higher field values than that 6T.

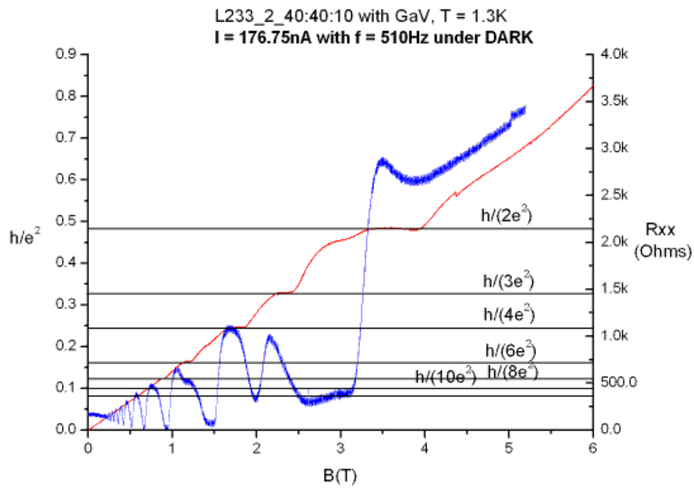
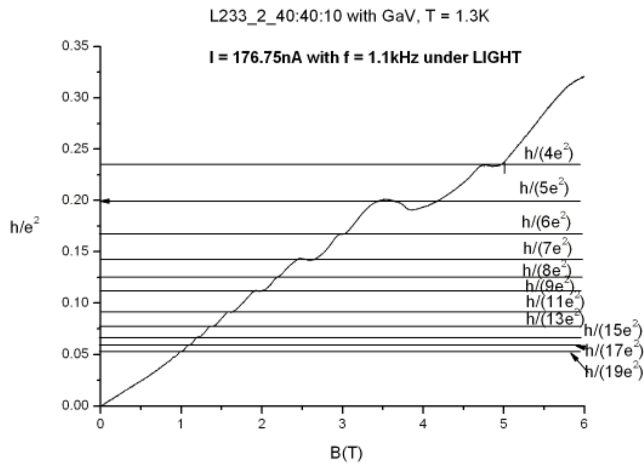



Figure 15. Quantized Hall Resistance for L 233 in Dark and Light shown in terms of Plateaux index as function of B (T)



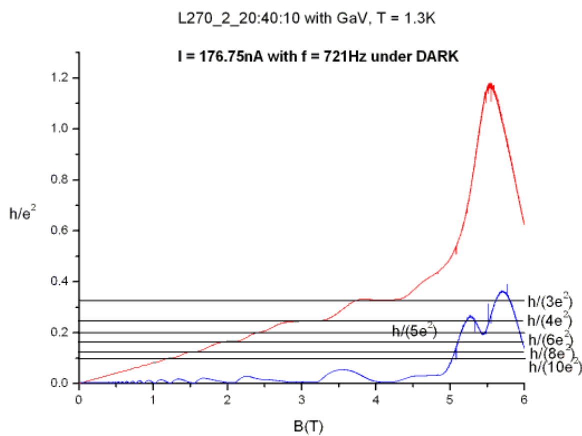
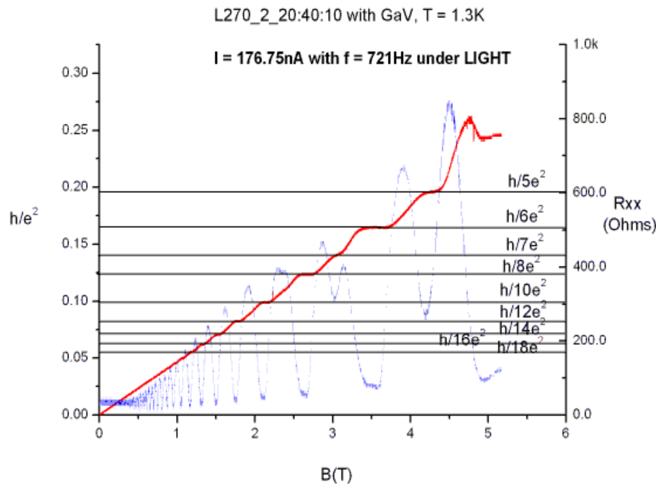




Figure 16. Quantized Hall Resistance for L 270 in Dark and Light, shown in terms of Plateaux index as function of B (T)




From the comments on the above plots it has been observed that for a 2DEG, the resistance is quantized at every 1/even multiples (i.e.1/2, 1/4, ..) of $h/ne^2$ at low magnetic field values and then finally the plateaux occur at every 1/integer multiples at high magnetic field values. However this is not the case when the electrons in the 2DEG layer are undergoing parallel conduction [14]. As one can see from Figure 17, for L 233 (40 nm spacer) structure, when the carriers were excited using illumination it resulted into conduction of carriers through a parallel channel as observed by quantum transport measurements. One of the important properties of parallel channel conduction is that, in the SdH oscillations observed the oscillations of the longitudinal voltage will not go back to zero point and as a result the quantized resistance plateaux does not essentially occur at the above predicted values under low and high magnetic field instead it will occur at random multiples. And this is the case which explains the plot of quantized resistance plateaux for L 233 under illumination conditions as shown in Figure 15.

Note the plot was not in format of data so wasn't shown from 0 to 6 T but instead shown from 6 to 0T.

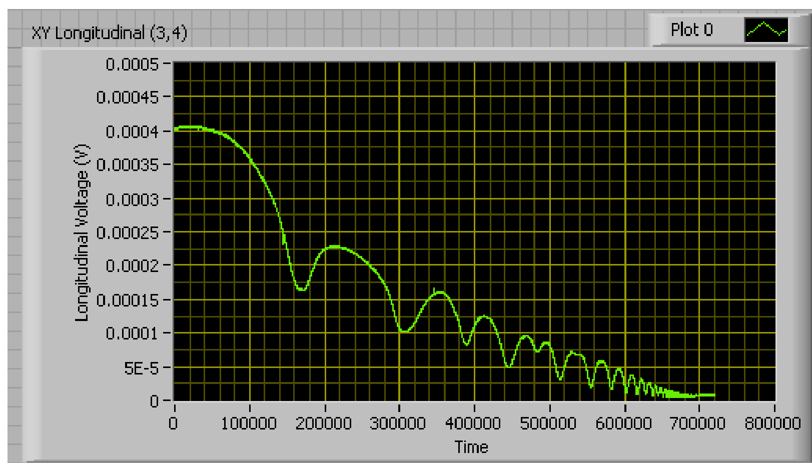



Figure 17. Quantized longitudinal voltage plotted for parallel conduction phenomena of 2DEG carriers

## QUASI-1D ELECTRON TRANSPORT:

In order to follow in the footsteps of previous research work carried out on conductance measurement of 1D split-gate devices, the point contacts as discussed

previously in were deposited on a 2DEG structure (L 270) of which sheet density measured is 2.93E11 ($cm^{-2}$) and mobility 815135.14 ($cm^2$/Vsec). After bonding 300 nm wide gap split-gate devices onto the chip package, setup for measurement was analyzed. The final setup designed for quasi-1D channel measurements is as shown in Figure 18.

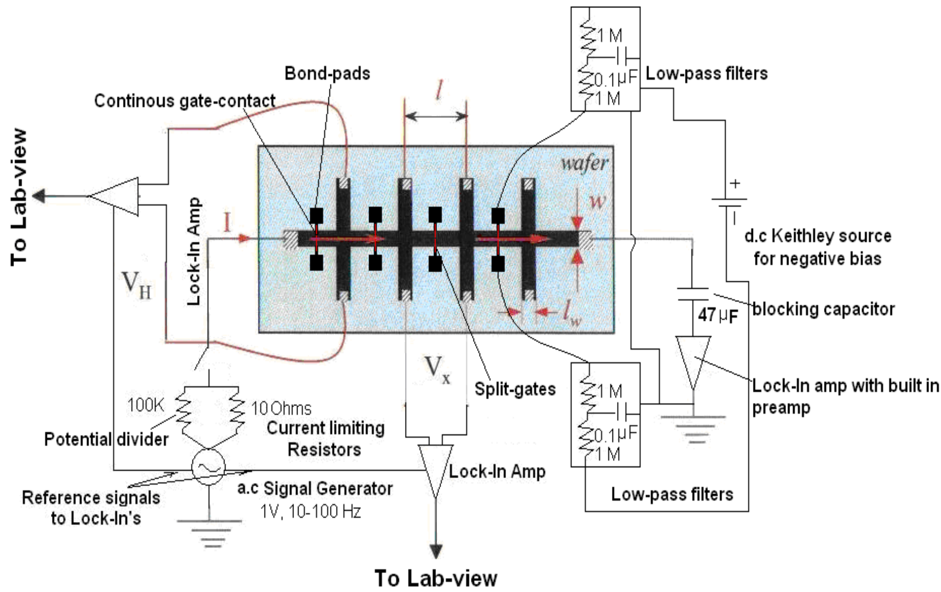



Figure 18. Final setup designed for quasi-1D transport measurements

In order to observe quantized conductance across the quasi-1D channel formed, 100 μV was applied across the Hall bar through potential divider circuit and the current from the other end of the hall bar was noted in order to see the channel effect on the flowing carriers. Hence when negative bias was applied across one of the four gates through low-pass filter it results into carrier depletion underneath the gate and this will limit the amount of current coming out on the other end of Hall bar. The channel depletion results, when negative bias up to 3 V applied to a split-gate is as shown in Figure 19.

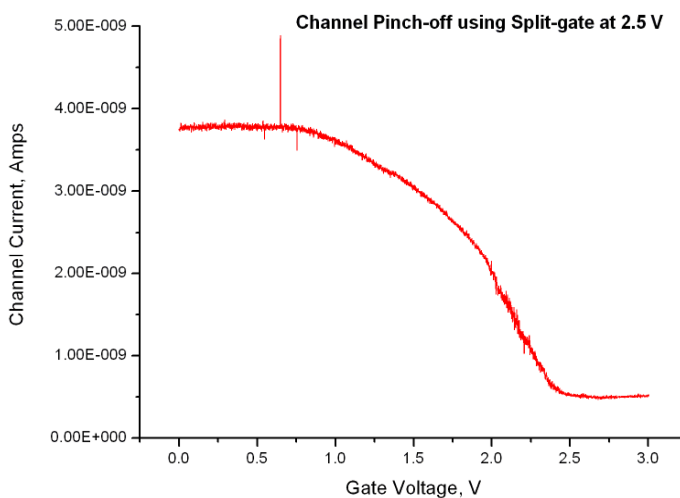



Figure 19. Plot of gate voltage vs channel current

As seen from Figure 19, the channel starts to deplete at gate bias of 0.1 V however further decrease in gate bias leads to channel pinch-off at around 2.5 V. These measurements were performed at 1.5 K, and this might be one reason for absence of conductance steps expected with respect to gate voltage. The reproducibility of the channel pinch-off was really good as well which gives positive indication for continuous overrun of split-gates on the mesa.

## CONCLUSION

The DC measurement for one batch of samples showed the sample with Ga to As ratio of 18% used, gave the highest mobility results.

The AC and DC analysis of different thickness spacer layer samples showed as by increasing the thickness, the sheet density in the sample decreases while the quality of the sample improves.

Fabrication and measurement techniques for quasi-1D channel defined in a 2DEG sample are successfully established.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REFERENCES

[1] Griebel M, Indlekofer K M, Forster A, Luth H 1999 *M Griebel et al J. Phys. D: Appl. Phys.* 32, 1729-33.

[2] Fowler A B, Hartstein A, Webb R A 1982 *Phys. Rev Lett.* 48, 196-99.

[3] Lee J and Vassell 1984 *J Lee et al J. Phys. C: Solid State Phys.* 17, 2525-35.

[4] Davies A G and Thompson 2007 *Advances in Nanoengineering: Electronics, Materials and Assembly, Imperial College Press.*

[5] Timp G, Chang A M, DeVegvar P, Howard R E, Behringer R, Cunningham J E and Mankiewich P 1988 *Surface Science* 196, 68-78.

[6] Mendez E E Price P J and Heiblum M 1984 *Appl. Phys. Lett.* 45, 3.

[7] Chandra A, Colin E C, Wood C, Woodard D W and Eastman L F 1978 *Solid-State Electronics* 22, 645-650.

[8] Harris J J, Foxon C T, Barnham K W J, Lacklison D E, Hewett J and White C 1986 *J. Appl. Phys.* 61, 3.

[9] Pepper M and Wakabayashi 1982 *J. Phys. C: Solid State Phys.* 15, L861-70.

[10] Mancoff F B, Zielinski L J, Marcus C M, Campman K, Gossard A C 1996 *Phys. Rev. B* 53, 12.

[11] Sharvin Yu V, Zh Eksp. Teor. Fiz. 1965 48, 984 *[Sov. Phys. JETP* 21, 665]

[12] Thornton T J, Pepper M, Ahmed H, Andrews D and Davies G J 1986 *Phys. Rev. Lett.* 56, 1198-1201.

[13] Barnes C H W, Cavendish Laboratory, University of Cambridge, *Quantum Electronics in Semiconductors.*

[14] Reed M A , Kirk W P and Kobiela P S 1986 *IEEE journal of Quantum Electronics* 22, 9.